
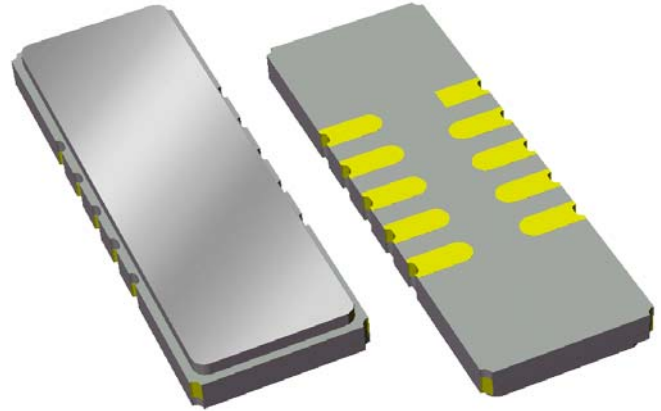


Preliminary Data Sheet

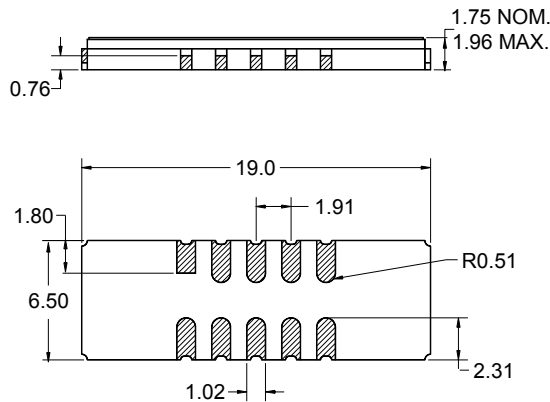
Features

- For broadband applications
- Typical 3 dB bandwidth of 3.0 MHz
- High attenuation
- Single-ended operation
- Ceramic Surface Mount Package (SMP)
- Replaces Sawtek P/N 851907 (BW 3dB=3.0 MHz)
- Hermetic
- RoHS compliant (2002/95/EC), Pb-free 



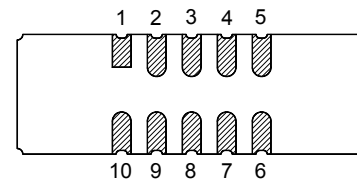
Package

Surface Mount 19.00 x 6.50 x 1.75 mm



Pin Configuration

Bottom View



Pin No.	Description
5	RF output
10	RF input
1,6	Ground
2,3,4	Case ground
7,8,9	Case ground

Dimensions shown are nominal in millimeters
 All tolerances are ± 0.15 mm except overall
 length and width $+0.15$ mm/ -0.10 mm

Body: Al_2O_3 ceramic
 Lid: Kovar, Ni plated
 Terminations: Au plating 0.5 - 1.0 μ m,
 over a 2 - 6 μ m Ni plating

Preliminary Data Sheet

Electrical Specifications ⁽¹⁾

Operating Temperature Range: ⁽²⁾ 0 to +70 °C

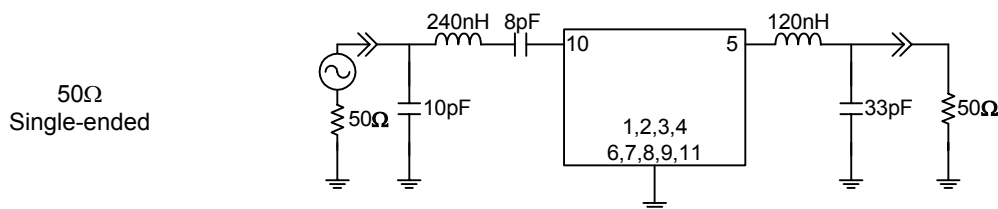
Parameter ⁽³⁾	Minimum	Typical	Maximum	Unit
Center Frequency	-	140	-	MHz
Minimum Insertion Loss	-	22.4	24	dB
Lower 1 dB Bandedge ⁽⁴⁾	-	138.60	138.71	MHz
Upper 1 dB Bandedge	141.31	141.43	-	MHz
Lower 3 dB Bandedge ⁽⁴⁾	-	138.43	138.505	MHz
Upper 3 dB Bandedge	141.495	141.61	-	MHz
Lower 40 dB Bandedge ⁽⁴⁾	137.57	137.70	-	MHz
Upper 40 dB Bandedge	-	142.36	142.43	MHz
Amplitude Variation 138.71 - 141.31 MHz	-	0.52	1.0	dB
Phase Linearity 138.71 - 141.31 MHz	-	1.84	4.35	deg
Group Delay Variation 138.71 - 141.31 MHz	-	42	115	nsec
Absolute Delay	-	2.02	-	μsec
Relative Attenuation ⁽⁴⁾				
10 - 80 MHz	50	66	-	dB
80 - 136 MHz	50	61	-	dB
144 - 200 MHz	50	55	-	dB
200 - 300 MHz	50	58	-	dB
Source Impedance: ⁽⁵⁾	-	50	-	Ω
Load Impedance: ⁽⁵⁾	-	50	-	Ω
Substrate Material	-	Quartz	-	-

Notes:

1. All specifications are based on the test circuit shown below
2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
3. Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances
4. All attenuation measurements are measured relative to minimum insertion loss
5. This is the optimum impedance in order to achieve the performance shown

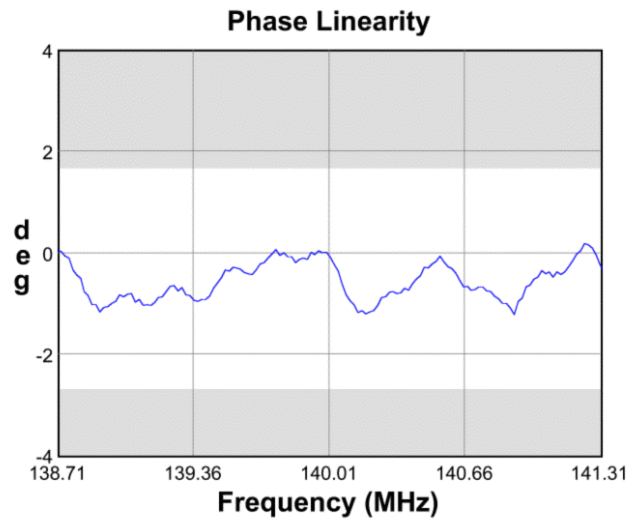
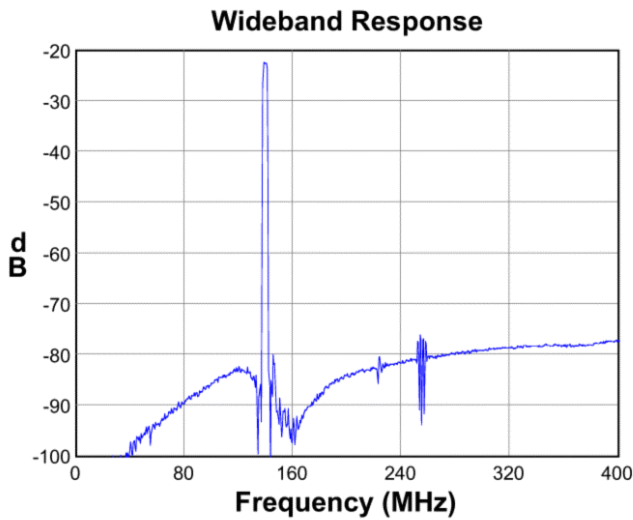
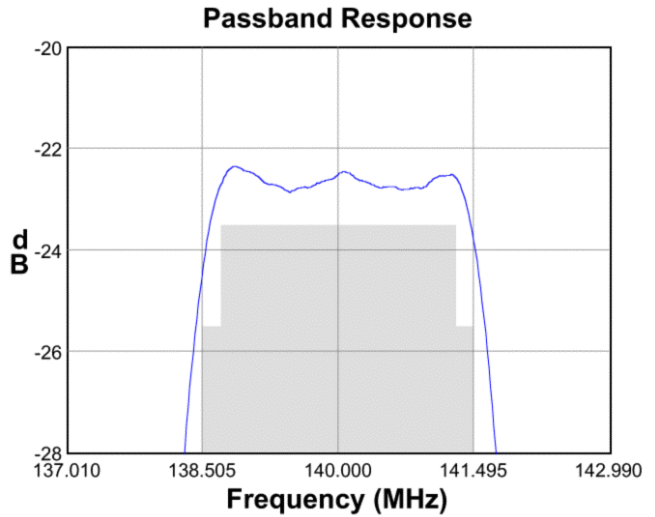
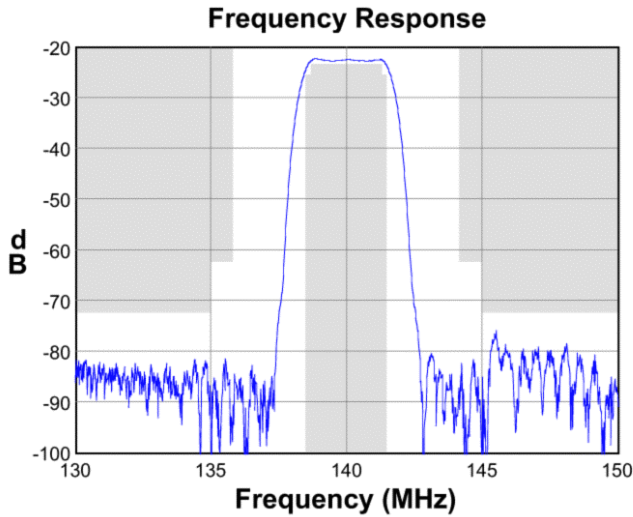
Test Circuit:

Actual matching values may vary due to PCB layout and parasitics

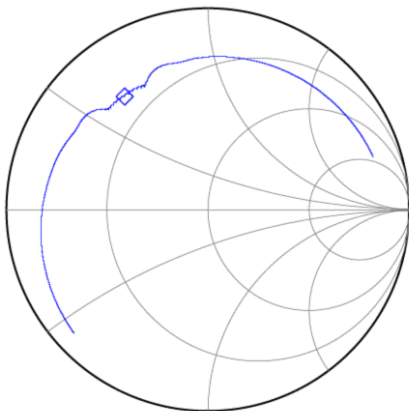


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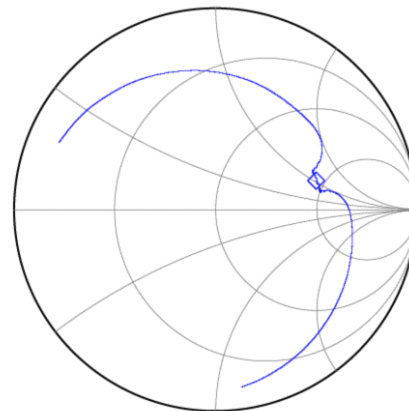
Typical Performance (at +25°C)



Input Smith Chart



Output Smith Chart




Preliminary Data Sheet

Maximum Ratings


Parameter	Symbol	Minimum	Typical	Maximum	Unit
Operating Temperature Range	T	0	+25	+70	°C
Storage Temperature Range	T _{stg}	-40	-	+85	°C

Important Notes

Warnings

- Electrostatic Sensitive Device (ESD) 
- Avoid ultrasonic exposure

RoHS Compliance

- This product complies with EU directive 2002/95/EC (RoHS) 

Solderability

- Compatible with JEDEC J-STD-020C **Pb-free** process, **260°C** peak reflow temperature ([see soldering profile](#))

Links to Additional Technical Information

[PCB Layout Tips](#)

[Qualification Flowchart](#)

[Soldering Profile](#)

[S-Parameters](#)

[RoHS Information](#)

[Other Technical Information](#)

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Contact Information



PO Box 609501
 Orlando, FL 32860-9501
 USA

Phone: +1 (407) 886-8860
 Fax: +1 (407) 886-7061
 Email: custservice@sawtek.com
 Web: www.sawtek.com

Or contact one of our worldwide
 Network of [sales offices](#),
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